



50

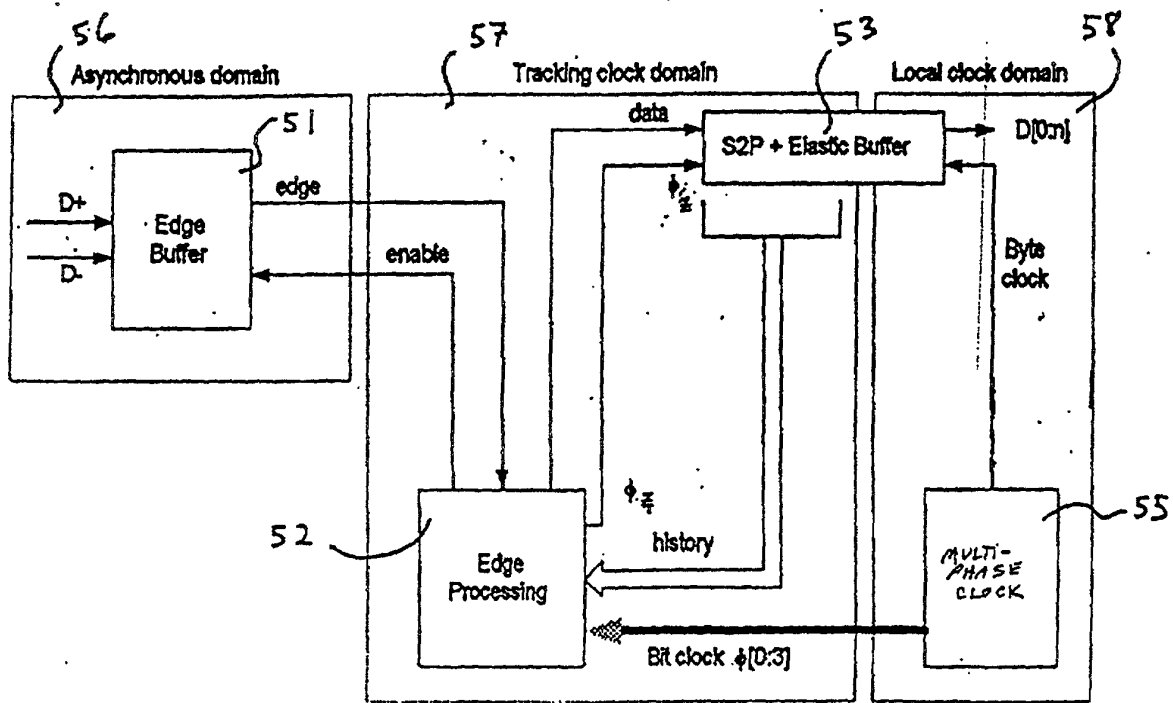
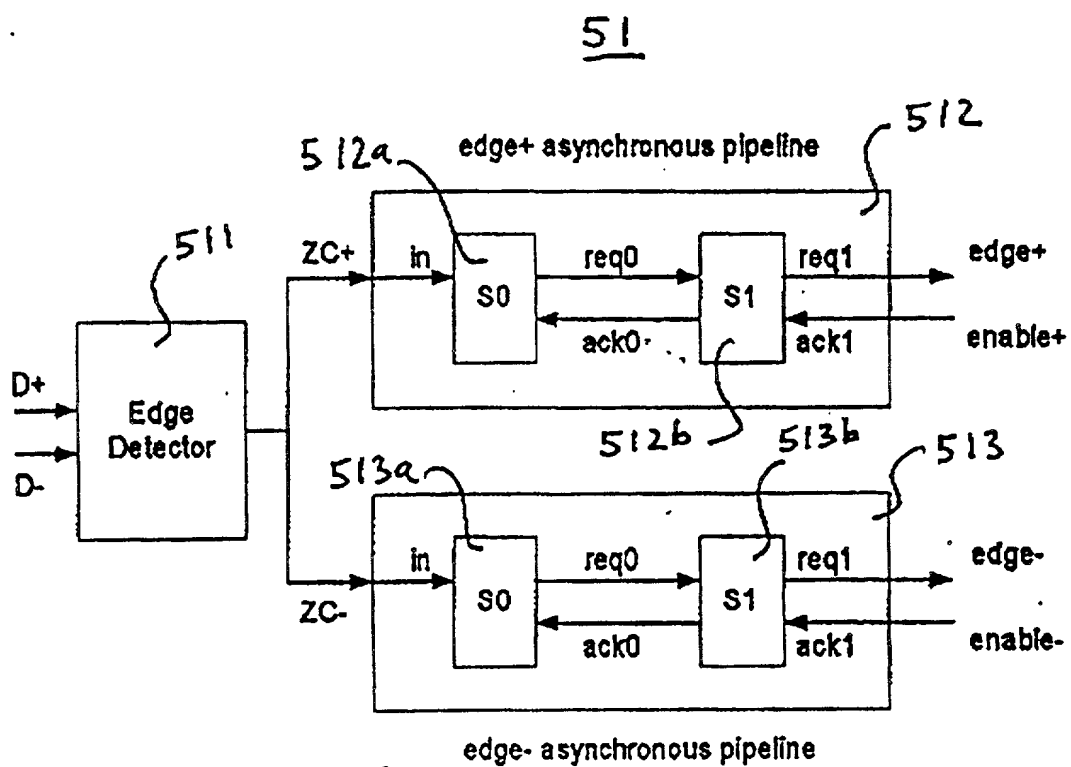
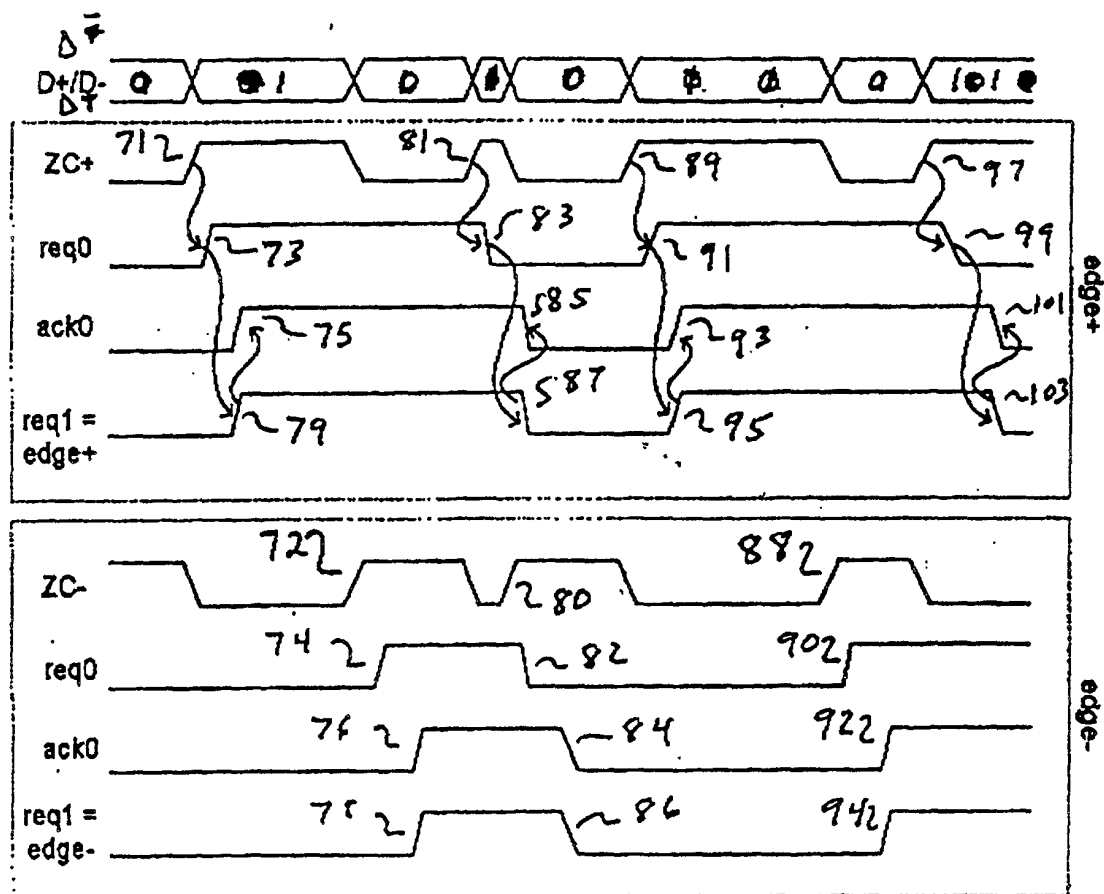


FIG 5  
Figure 1-1: High Level Block Diagram of Edge Based Receiver.



6  
Figure 1-2: Edge Buffer Block Diagram.



7  
Figure 1-3: Timing Diagrams for the Edge Pipelines.

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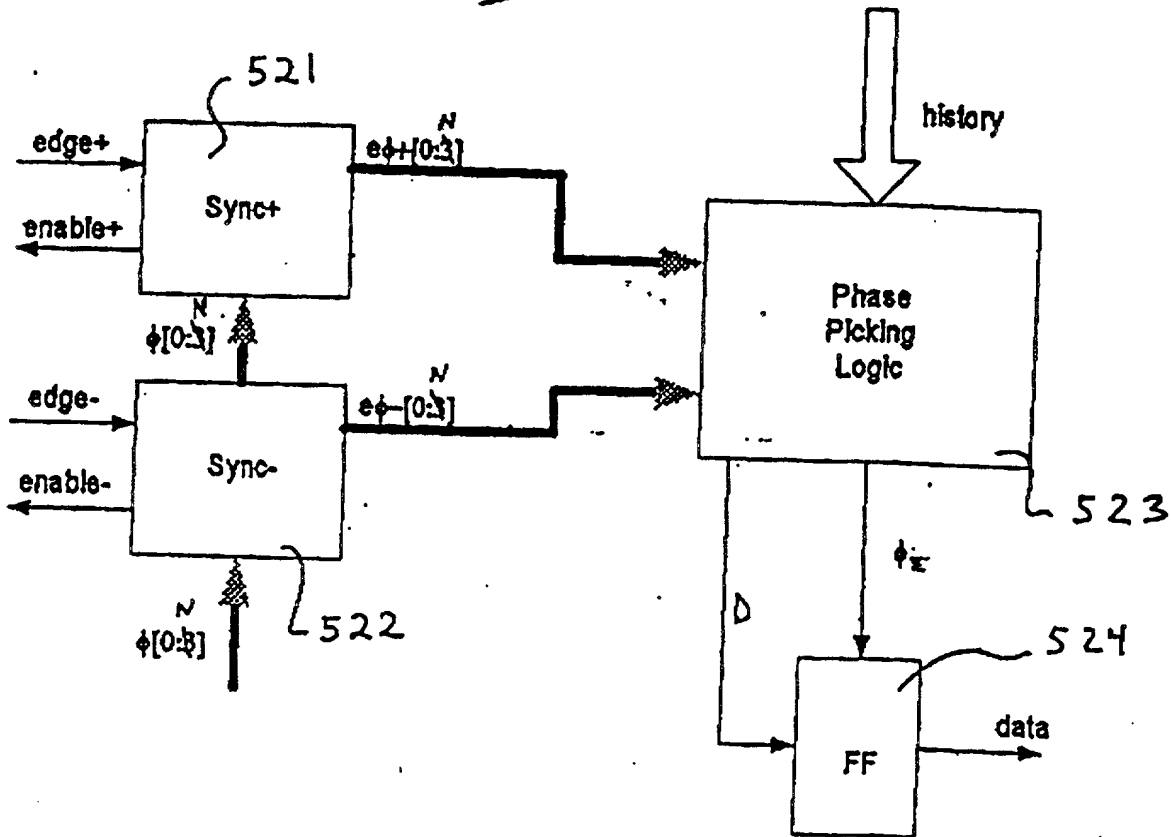


Figure 1-5: Edge Processing Block Diagram.

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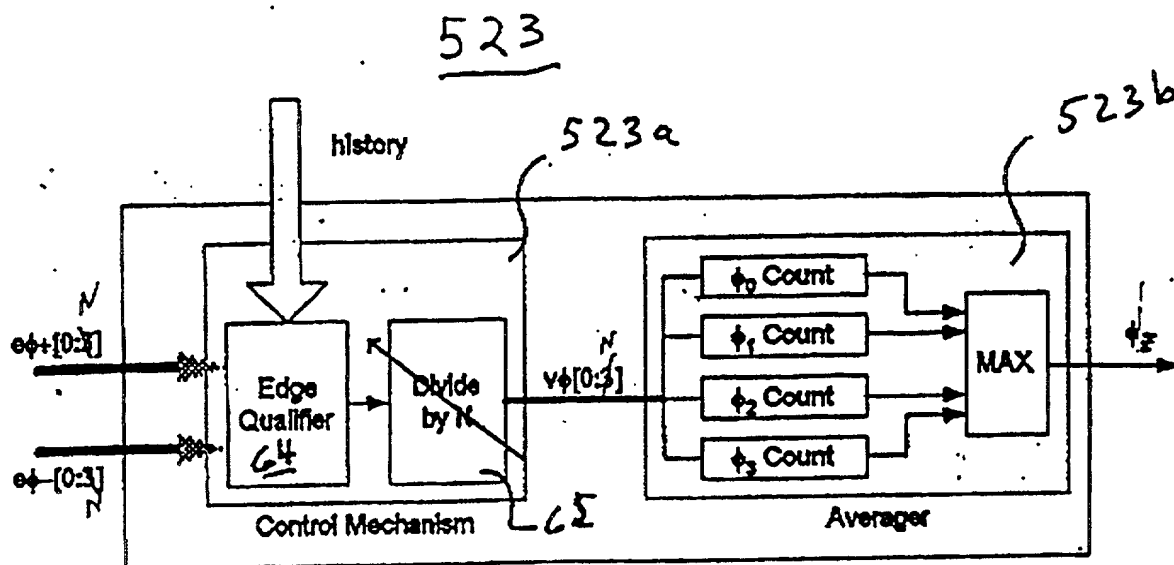
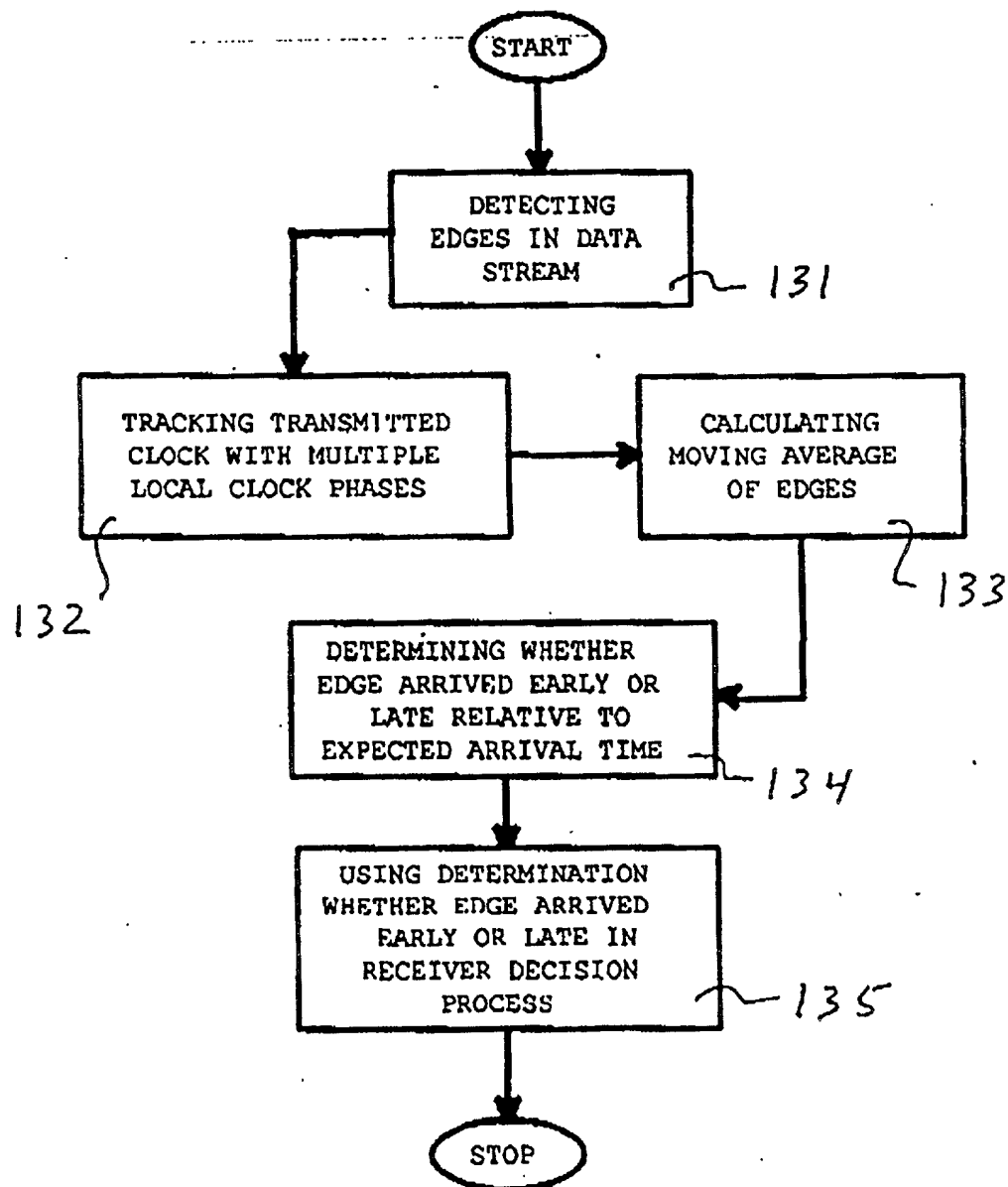


Figure 1-7: Phase Picking Mechanism Block Diagram.

FIG 11



005737 043 432900



FIG 12a

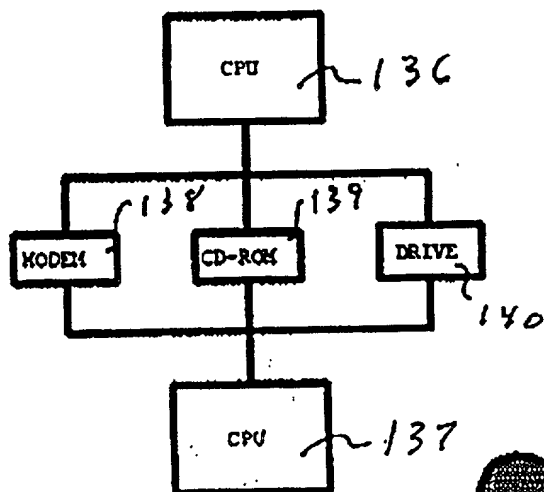


FIG 12b

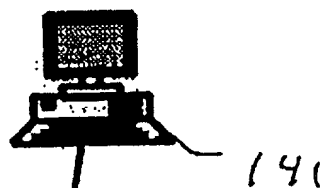


FIG 12c

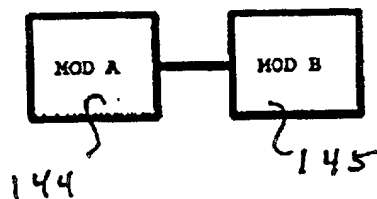
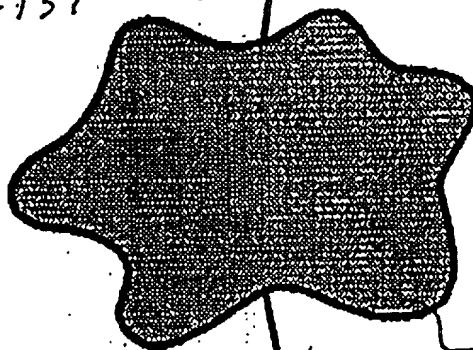
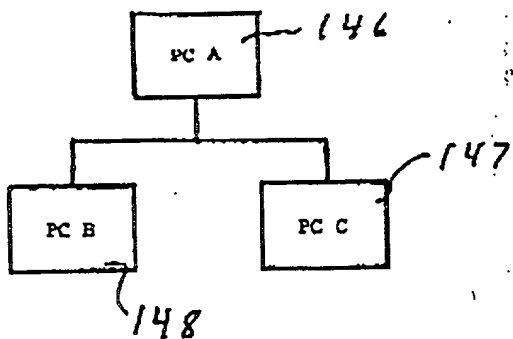


FIG 12d



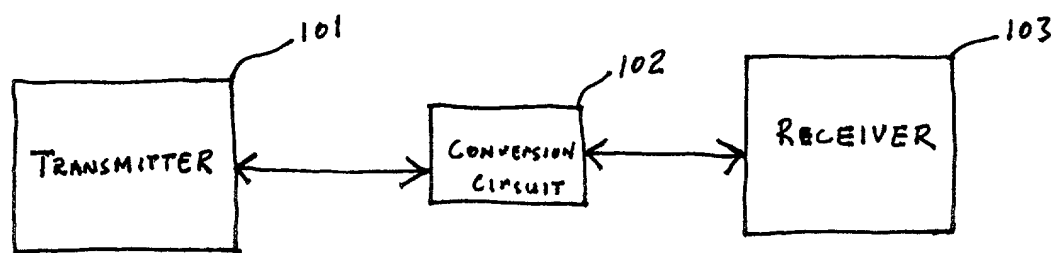


FIG. 13

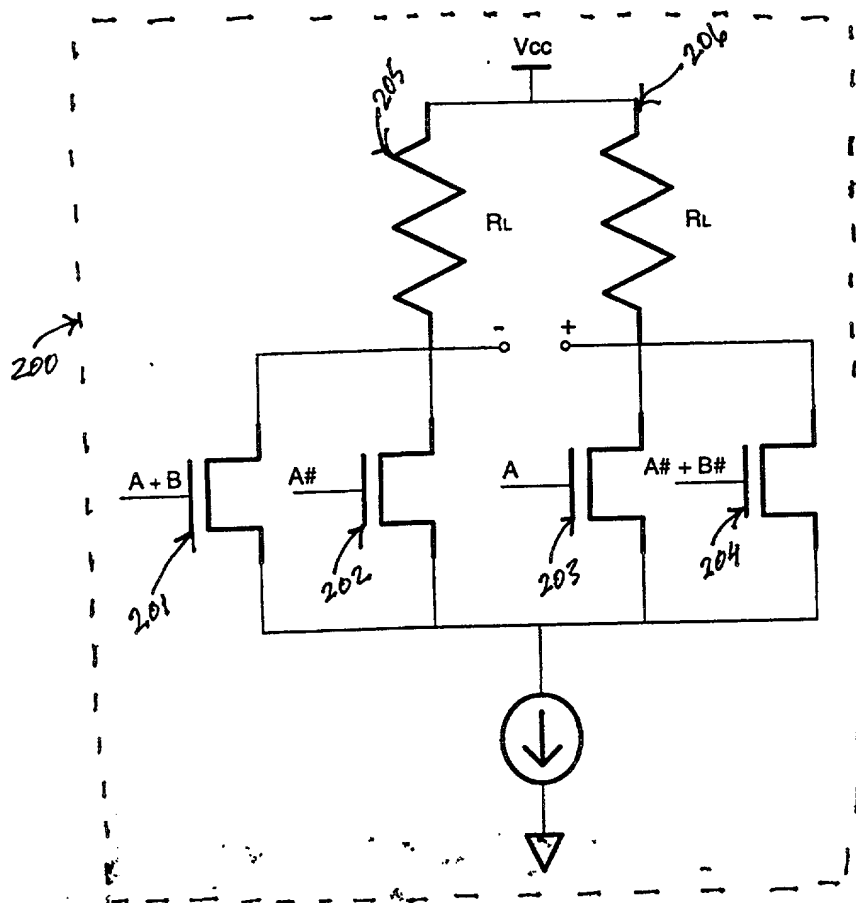
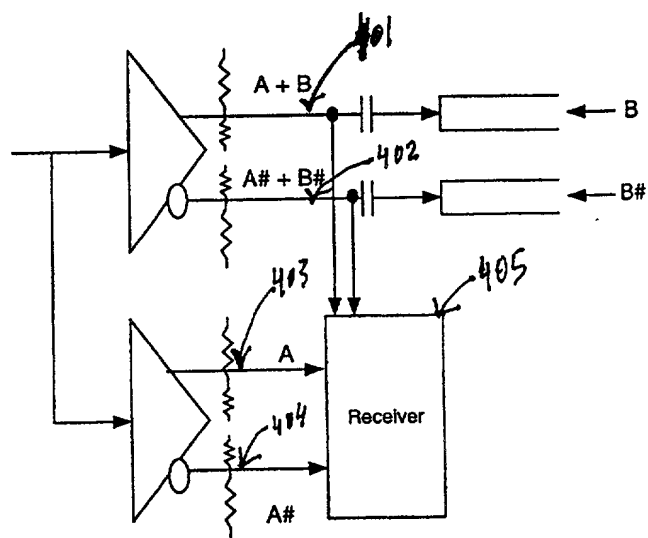
[illegible]

FIG 14

Signals	A	A#	B	B#	A + B	A# + B#	High Out
Actual Volt.	1.0V	0.5V	0.25V	-0.25V	1.25V	0.25V	+
			-0.25V	0.25V	0.75V	0.75V	-
			0.05V	-0.05V	1.05V	0.45V	+
			-0.05V	0.05V	0.95V	0.55V	-
			0V	0V	1.0V	0.5V	tie
	0.5v	1.0v	0.25V	-0.25V	0.75V	0.75V	+
			-0.25V	0.25V	0.25V	1.25V	-
			0.05V	-0.05V	0.55V	0.95V	+
			-0.05V	0.05V	0.45V	1.05V	-
			0V	0V	0.5V	1.0V	tie

**FIG 15**

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006037-6735260



**FIG 16**